Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"systolic memory array" and "off-die"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 10:42
L2	1	systolic same memory same array and "off-die"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 10:42
L3	1	systolic same memory same array and (off same die)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 10:42
L4	12	systolic same memory same array and die	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 10:55
L5	3555	((systolic same memory same array) SMA) and peripheral$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 10:56
L6	324	((systolic same memory same array) SMA) and peripheral$1 same ("one side" "same side")	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 10:56
L7	324	("systolic memory array" SMA) and peripheral$1 same ("one side" "same side")	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 12:38
L8	245	("systolic memory array" SMA) and peripheral$1 and 7$2/$3.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 10:59
L9	1	"systolic memory array" and peripheral$1 and 7$2/$3.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 11:00
L10	1	systolic same "memory array" and peripheral$1 and 7$2/$3.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 11:01
L11	3	systolic same "memory array" and peripheral$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 11:02
L13	872	"pipeline stages" same cycles	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 11:07
L20	207	number near2 "pipeline stages" same cycles	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 11:07
L21	1	"systolic memory array" and peripheral$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 13:16
L23	3	systolic same "memory array" and peripheral$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 13:16

L24	4	systolic same "memory array" same access	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 14:05
L25	42	"memory array" same peripheral$1 same "one side"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 14:05
S1	74	memory same arrays same pipeline$1 same architecture	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/06 13:17
S2	1	memory same arrays same pipeline$1 same architecture and systolic.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/06 13:13
S3	140	systolic.ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/06 13:16
S4	2	(systolic and memory).ti.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/06 13:16
S8	22	memory same arrays same pipeline$1 same order same processing	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/06 13:18
S9	9	memory near2 arrays same pipeline$1 same order same process$4	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/06 13:19
S10	77	arrays same pipeline$1 same systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/09 15:40
S33	7	arrays same pipeline$1 same apparatus same architecture	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/09 15:41
S34	32	arrays same pipeline$1 same microprocessor same order	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/09 16:57
S35	19	arrays same pipeline$1 adj processor same memory	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 11:08
S36	5	arrays same banks same pipeline$1 same processor same memory	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 09:44
S38	7	arrays same pipeline$1 adj processor same memory and "out-of-order"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 10:54
S42	2	arrays same processor same die same network same memory	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 11:05
S43	15	arrays same die same network same memory	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 11:05

S45	5	arrays same banks same pipeline$1 same processor same memory	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 11:10
S46	20	"memory arrays" same banks same pipeline$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 11:12
S47	59	arrays same memory same banks same pipeline$3	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 15:22
S49	2	arrays same memory same banks same frequency same width	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 15:22
S51	15	arrays same memory same banks same frequency	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 15:43
S54	1	arrays same memory same banks and frequency same width same pipeline	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 15:47
S55	44	arrays same memory same banks and frequency same width	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 15:47
S56	9	arrays same memory same banks and frequency same width and stages same cycles	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 16:04
S57	82	arrays same memory same banks and (stages same cycles)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 16:49
S58	1	arrays same memory same banks and (stages same cycles) and (pump$3 same address same cycle)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 16:31
S59	4	arrays same memory same banks and (pump$3 same address same cycle)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 16:28
S60	16	arrays same memory same banks and ("pipeline stages" same cycles)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 16:34
S61	36	arrays same banks and ("pipeline stages" same number same cycles)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 16:46
S70	69	(pipeline$1 adj stage$1 same cycles same ("equal" "same as"))	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 16:55
S71	7	(pipeline$1 adj stage$1 same cycles same ("equal" "same as")) and arrays same banks	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 17:18
S74	1	"address pipe" same pump$3 same address$3	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 17:19

S75	1	pump$3 adj2 address$3 same banks same cycle$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/10 17:19
S76	22	pump$3 same address$3 same banks same cycle$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 10:10
S77	42	array$1 same banks same interleaved same addresses	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 10:21
S78	102	array$1 same banks same interleaved same address$3	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 10:24
S79	52	arrays same banks same interleaved same address$3	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 10:25
S80	141	arrays same memory same interleaved same address$3	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 10:33
S81	188	arrays same memory and banks same interleaved same address$3	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 11:01
S83	49	arrays same memory same banks and interleaved same address$3 same different	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 11:09
S84	44	arrays same memory same banks same interleaved same address$3	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 11:12
S85	2	arrays same memory same banks same interleaved same address$3 same eight	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 11:10
S86	107	arrays same banks same interleav$3 same address$3	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 12:02
S89	7	arrays same eight same banks same interleav$3 same address$3	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 12:43
S90	2	apparatus same pipeline$1 same architecture same arrays same microprocessor	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 12:44
S91	7	apparatus same pipeline$1 same architecture same arrays	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 12:45
S92	47	apparatus same pipeline$1 same arrays	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 14:20
S93	1	apparatus same pipeline$1 same arrays same systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 14:20

S94	77	pipeline$1 same arrays same systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 15:18
S96	1	pipeline$1 same arrays same banks same systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 14:58
S97	5	pipeline$1 same arrays same memory same systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 15:14
S98	57	pipeline$1 near3 arrays same (processor$1 microprocessor$1)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 15:24
S99	81	pipeline$1 near3 arrays and pipeline$1 near3 (processor$1 microprocessor$1)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 15:26
S100	106	pipeline$1 near5 arrays and pipeline$1 near3 (processor$1 microprocessor$1)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/11 15:30
S101	9	pipelined near2 arrays and pipelined near2 (processor$1 microprocessor1)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:02
S102	161	pipelined same arrays same (processor$1 microprocessor1)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:02
S103	1	pipelined same arrays same (banks "sub-arrays") same (processor$1 microprocessor1)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:02
S104	1	pipelined same arrays same banks same (processor$1 microprocessor1)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:02
S105	161	pipelined same arrays same (processor$1 microprocessor1)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:03
S106	14	pipelined same "memory arrays" same (processor$1 microprocessor1)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:33
S107	440	pump$3 same address$3 same write$2 same memory	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:34
S108	14	pumping same address same write same memory	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:39
S109	11	pumping same address same read same memory same cycle	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:40
S110	6	pumping same address same read same write same cycle	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:40

S111	33	pump$3 same address same read same write same cycle	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 11:51
S112	59	pump$3 same address same read same cycle	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 12:16
S113	736	pipelined near2 microprocessor	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 12:16
S114	2	"pipelined microprocessor" and arrays same banks same memory	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 12:17
S115	28	"pipelined microprocessor" and arrays same banks	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 12:19
S116	8	"pipelined microprocessor" and "memory arrays"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 15:35
S117	10	"pipelined stages" same "clock cycles"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 16:59
S118	0	"pipelined stages" same cycles same latency same throughput	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 17:00
S119	8	"pipelined stages" same latency same throughput	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 17:00
S120	132	pipeline$1 same stages same latency same throughput	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/12 17:02
S121	8	pipeline$1 same stages same latency same throughput and frequency same (width bandwidth)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:03
S122	0	pipeline$1 same stages same "number of"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:04
S123	2115	pipeline$1 same stages same cycles	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:04
S124	899	pipeline$1 adj1 stages same cycles	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:05
S125	18	"pipeline stages" same cycles same bank$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:16
S126	20	"2i+L"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:16

S127	374	"pipeline stages" same cycles same number	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:22
S128	198	"pipeline stages" same "clock cycles" same number	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:23
S129	0	"pipeline stages" same "clock cycles" same "same as" same number	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:23
S130	0	"pipeline stages" same "clock cycles" same "same as"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:24
S131	198	"pipeline stages" same "clock cycles" same number	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:29
S132	0	"pipeline stages" same "number of clock cycles"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:29
S133	0	"pipeline stages" same "number of cycles"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:29
S134	48	pipeline$1 adj1 stages same cycles same equal	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:35
S135	0	"peripheral access" same "systolic array"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:35
S136	1	peripheral$1 same "systolic array"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:35
S137	1	"one side" same "systolic array"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:38
S138	3	"systolic array" same periph$4	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:38
S139	3	"systolic array" same periph$5	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 11:40
S140	525	"systolic array"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 17:15
S141	1	pump$3 same address same pipe same cycle same bank	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 12:24
S142	5	pump$3 same address same pipe same cycle	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 12:24

S143	31	pump$3 same address same cycle same bank	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 10:30
S144	18	"systolic array" same side	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 17:17
S147	3	systolic same array same "one side"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 17:19
S148	6	systolic same array same periph$5	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/18 17:19
S149	32	pump$3 same address$2 same cycle$1 same bank$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 10:30
S150	4148	address$2 same cycle$1 same bank$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 10:47
S152	275	address$2 same "one cycle" same bank$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 10:53
S154	8	address$2 same "one cycle" same individual same bank$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 10:55
S155	1	"address pipe" same cycle same bank$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 10:56
S156	9	address same pipe same cycle same bank$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 11:05
S157	6	address same pipe same cycle same bank$1 same writ$4	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 15:46
S158	0	latency same "2i+"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 15:46
S159	1	latency same "2 i +"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 15:47
S160	1	latency same "2i+l"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 15:47
S162	122	latency same cycles same time same address same bank	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 15:51
S163	0	"2i + L"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 15:51

S164	15	"access latency" same represented	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 15:55
S165	11	"access latency" same address same bank same cycles	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 17:14
S166	1	"access latency" same address$2 same bank$1 same cycle$1 and systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 16:02
S167	4	access same (time latency) same address$2 same bank$1 same cycle$1 and systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 16:02
S168	4	access same (delay time latency) same address$2 same bank$1 same cycle$1 and systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/20 10:41
S170	86	"one side" same systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 16:29
S171	1	"peripheral access" same "systolic memory array"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 16:24
S172	1	peripheral$1 same "systolic memory array"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 16:25
S177	42	"one side" same "memory array" same peripheral$1	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 16:43
S178	1	"memory array" same "peripheral access"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 16:30
S179	7	"peripheral access" same "one side"	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 16:31
S180	1	"memory array" same peripheral$1 and systolic	US-PGPUB; USPAT; USOCR	OR	OFF	2006/01/19 16:43